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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,644	05/19/2004	Mark D. Dupuis	BUR920040106US1	3643

30449 7590 12/13/2005

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AJC

Office Action Summary	Application No.	Applicant(s)	
	10/709,644	DUPUIS ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-32* is/are allowed.

6)☒ Claim(s) *1-27 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 10/04/05, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 8-11, 14, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiota (US 2002/0115228).

With reference to Figs. 27-29 in conjunction with Fig. 1, the reference teaches the claimed invention in that it discloses a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first region **60** of single crystalline Si (*it is inherent that the silicon substrate **60** is of single crystalline because the grown **epitaxial** layer **81** is of single crystalline*) and a second region **61** of insulating material, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface (Fig.27) , and

(ii) depositing SiGe simultaneously on top of the first and second regions so as to grow third region **81** of single crystalline SiGe and fourth region **80** of polycrystalline SiGe from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows

from the first common interface surface, wherein the first and third regions comprise a same material (i.e., silicon) and have single-crystal atoms arrangement, wherein the first region has a different atoms arrangement than the fourth region (*single crystalline has different atoms arrangement than polycrystalline*), and wherein the step of depositing the growth material is performed under a first deposition condition (Fig. 28 and para. [0104]).

Note that, although Fig. 28 shows a single semiconductor structure, it is understood that the batchwise processing of the prior art involves the formation of a plurality of semiconductor structures identical to Fig. 28 in the same wafer. Furthermore, in paragraph [0109], the prior art discloses "The film quality controlling method according to this invention is effective also for the process using non-selective growth over the entire surface". And the film quality controlling method is illustrated in Fig. 1 and described in paragraph [0066]. That is, the method described above further includes the following step:

iii) if the first thickness and composition of the thin film grown on the substrate (*corresponding to the claimed first yield*) is different from the desired one (*i.e., not within a pre-specified range of a target yield*), the film growth conditions are re-designed, and the thin film is grown in the next batch under the redesigned conditions (*i.e., repeating step (a)(i) and (a)(i) in the next batch, except that the step of depositing the growth material is performed under a second depositing conditions*). See Fig. 1, paragraph [0066], and claim 11.

For claims 2 and 15, Fig. 1 includes a condition in which a second yield is different from the desired one (target yield) then forming a third plurality of semiconductor structures identical to Fig. 28 in the next batch under the redesigned conditions (*i.e., repeating step (a)(i) and (a)(i) in the next batch, except that the step of depositing the growth material is performed under a third depositing conditions*).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyota as above.

Kiyota teaches a method as described above. Kiyota differs from the claims in not specifically disclosing that the first yield of the first plurality of identical semiconductor structures is a function of a percentage of satisfactory structures of identical semiconductor structure in all the first plurality of identical semiconductor structures. However, Hiyota in paragraph [0066] discloses that "When the result is satisfactory (OK), thin films are grown under the same conditions in and after the next batch". Thus, one of ordinary skill in the art would find it obvious that the desired growth conditions that result in thin films having desired thickness and composition

(first yield) would be determined by the high percentage of satisfactory structures of identical structure in all the first plurality of identical structure in the same wafer. Such determination would ensure the film growth process can be controlled precisely to decrease any variation of the film thickness between each of the wafers, and therefore increase yield.

6. Claims 12-13, 21-22, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyota as above in view of Emons et al. of record.

Kiyota teaches a batchwise processing as described above. Kiyota differs from the claims in not disclosing the steps of forming a single-crystal silicon on the silicon substrate 60; and growing a seed layer of polysilicon on top of the first and second shallow trench isolation region 61 as recited in claim 21.

In the same field of endeavor, Emons teaches a method of forming a heterojunction bipolar transistor in which a thick single-crystal epitaxial layer 3 is formed on a silicon substrate, and the method further includes the step of forming a seed layer 4 of polysilicon on top of isolation regions 8 prior to the step of growing simultaneously single crystalline SiGe layer 1A and polycrystalline SiGe layer 1B (Fig. 3, col. 3, lines 65-66; col. 4, lines 1-5, col. 5, lines 6-9).

It would have been obvious to one of ordinary skill in the art to modify Kiyota's teaching by forming a thick single-crystal silicon layer on the substrate 60 and forming a polysilicon seed layer on top of isolation regions 61 as suggested by Emons because

the use of the thick single-crystal silicon layer would ensure to accommodate thick isolation region and the use of the polysilicon seed layer would enhance the uniform growth of the SiGe layer 80.

For claim 22, Fig. 1 of Kiyota includes a condition in which a second yield is different from the desired one (target yield) then forming a third plurality of semiconductor structures identical to Fig. 28 in the next batch under the redesigned conditions (*i.e., repeating step (a)(i) and (a)(i) in the next batch, except that the step of depositing the growth material is performed under a third depositing conditions*).

For claim 35, Hiyota in paragraph [0066] discloses that "When the result is satisfactory (OK), thin films are grown under the same conditions in and after the next batch". Thus, one of ordinary skill in the art would find it obvious that the desired growth conditions that result in thin films having desired thickness and composition (first yield) would be determined by the high percentage of satisfactory structures of identical structure in all the first plurality of identical structure in the same wafer. Such determination would ensure the film growth process can be controlled precisely to decrease any variation of the film thickness between each of the wafers, and thusly increasing yield.

7. Claims 3-7, 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyota as above in view of U'Ren (US 6,365,479).

Kiyota teaches a batchwise processing as described above. Kiyota differs from

the claims in not disclosing that the adjustment of the growth conditions for making the film of the next batch is performed in the manner as recited in the claims.

In the same field of endeavor, U'Ren recognizes that physical properties such as thickness and concentration of a SiGe single-crystal base and a SiGe polycrystalline base contact are important in the making of a SiGe HBT (col. 2, lines 1-10). According, U'Ren teaches a process for controlling the thickness/concentration of the SiGe single-crystal base and the SiGe polycrystalline base contact by controlling the deposition process parameters such as temperature (T), pressure (P), and precursor gas flow rate (F) (see col. 4, lines 59-67; col. 7, lines 64-67; col. 8, lines 15-25; col. 9, lines 35-67).

It would have been obvious to one of ordinary skill in the art to modify Kiyota's teaching by adjusting the growth conditions for depositing the thin film of the next batch by controlling process effective variables such as T, P and/or F so that a film of a desired thickness and composition can be obtained. The SiGe single-crystal base and the SiGe polycrystalline base contact having desired thickness and composition would optimize the performance of the SiGe HBT device as suggested by U'Ren.

As for the controlling of T, P and/or F in the manner recited in the claims, such would have been obvious to one skilled in the art because it has been held that discovery of an optimum value of a result-effective variable in a known process involves only routine skilled in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

8. Claims 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyota taken with Emons as applied to claims 12-13, 21-22, and 35 above, and further in view of U'Rent cited above.

The combination of Kiyota and Emons teaches the batchwise processing as described above. The combined process differs from the claims in not disclosing that the adjustment of the growth conditions for making the film of the next batch is performed in the manner as recited in the claims.

In the same field of endeavor, U'Ren recognizes that physical properties such as thickness and concentration of a SiGe single-crystal base and a SiGe polycrystalline base contact are important in the making of a SiGe HBT (col. 2, lines 1-10). According, U'Ren teaches a process for controlling the thickness of the SiGe single-crystal base and the SiGe polycrystalline base contact by controlling the deposition process parameters such as temperature (T), pressure (P), and precursor gas flow rate (F) (see col. 4, lines 59-67; col. 7, lines 64-67; col. 8, lines 15-25; col. 9, lines 35-67).

It would have been obvious to one of ordinary skill in the art to modify the combined process by adjusting the growth conditions for depositing the thin film of the next batch by controlling process effective variables such as T, P and/or F so that a film of a desired thickness and composition can be obtained. The SiGe single-crystal base and the SiGe polycrystalline base contact having desired thickness and composition would optimize the performance of the SiGe HBT device as suggested by U'Ren.

As for the controlling of T, P and/or F in the manner recited in the claims, such would have been obvious to one skilled in the art because it has been held that discovery of an optimum value of a result-effective variable in a known process involves only routine skilled in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Allowable Subject Matter

9. Claims 28-32 are allowed over prior art of record.

10. The following is an examiner's statement of reasons for allowance:

Claim 28 and its dependent claims are allowed because the prior art does not teach or suggest the claimed step of determining a desired deposition temperature and a desired precursor flow rate based on the target yield and the relationship between a yield of the semiconductor structure design, a deposition temperature, and a precursor flow rate, wherein the yield of the semiconductor structure design is a function of a percentage of satisfactory structures of a plurality of semiconductor structures formed according to the semiconductor structure design in all the plurality of semiconductor structures.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

12/12/05

Notice of References Cited	Application/Control No. 10/709,644	Applicant(s)/Patent Under Reexamination DUPUIS ET AL.	
	Examiner Trung Dang	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0115228	08-2002	Kiyota, Yukihiro	438/7
*	B	US-6,365,479	04-2002	U'Ren, Gregory D.	438/320
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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